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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,620	09/25/2003	Jeffrey C. Swanson	10002929-3	6729

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EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,620	SWANSON ET AL.	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17,18 and 20* is/are allowed.

6)☒ Claim(s) *1-16 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/15/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final Office Action

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-17 of U.S. Patent No. 6,662,313 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

Claim(s) 1-17 of patent 6,662,313 B1 contain(s) every element of claim(s) 1-21 of the instant application and as such anticipate(s) claim(s) 1-21 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-3, 12-16, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ranson et al., U.S. Patent 5,867,644.

Referring to claim 1:

a. In column 28, lines 57-64, Ranson et al. disclose that various 16:1 multiplexers are physically located at various remote locations around the microprocessor. Each has its inputs coupled to a set of test nodes (a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit).

b. In column 15, lines 44-67 continued in column 16, lines 1-5, Ranson et al. disclose that the four bits of present state bus are provided to one of the inputs of comparator so that they may be compared with the contents of storage element, which specifies the present state during which entry will become active (a trigger event generator receiving a first N bits of sampled data from said network). The four bits that are output from the comparator are ANDed together at AND gate, yielding a one-bit match result for present state. Similarly, the contents of storage element 1202 are compared with the eleven bits of state machine input bus by the comparator. An OR gate is used to mask the output bits of the comparator with the contents of the storage element. The results of this masking operation are ANDed together, resulting in a match result for the state machine input bus (said trigger event generator including a definable mask and selectively performing a Boolean operation on said sampled data based on said mask to provide a trigger event).

c. In Figure 4 and in column 13, lines 38-67 continued in column 14, lines 1-62, Ranson et al. teach a FIFO storage array that stores at least a portion of the sampled data.

Referring to claim 2:

a. In column 15, lines 44-57, Ranson et al. disclose the four bits that are output from the comparator are ANDed together at AND gate, yielding a one-bit match result for present state (a result of said Boolean operation on said sampled data).

b. In column 3, lines 55-58, Ranson et al. disclose that the outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times (a performance counter event signal).

c. In the Abstract, Ranson et al. disclose that the output devices also include circuitry for generating internal and external triggers (an externally applied trigger signal).

Referring to claim 3, in column 3, lines 55-58, Ranson et al. disclose that the outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times (a counter providing an intermediate trigger in response to a predetermined number of said trigger events).

Referring to claim 12, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors the external pulse signal (a sampling circuit responsive to said trigger command to identify target data).

Referring to claims 13 and 14, in columns 16-26, Ranson et al. disclose sample-on-the-fly circuitry that latches the state of the test nodes 0-n whenever a control signal is asserted. Specifically in column 23, lines 60-67, Ranson et al. disclose storing only certain data matches (a first and second N bits of sampled data supplied by said network).

Referring to claim 15, in Figure 4, Ranson et al. disclose remote registers for storing the data (said sampling circuit includes a memory storing said target data).

Referring to claim 16, in column 11, lines 16-26, Ranson et al. disclose sample-on-the-fly circuitry that latches the state of the test nodes 0-n whenever a control signal is asserted (switching circuitry configured to selectively provide a predetermined portion of said target data).

Referring to claim 19, in Figure 4, Ranson et al. disclose a storage array in which the bits are shifted serially through the remote registers (wherein said sampling circuit includes a FIFO storage array).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ranson et al., U.S. Patent 5,867,644 as applied to claim 1 above, and further in view of Tobin et al., U.S. Patent 5,771,240.

Referring to claims 4 and 10, in column 3, lines 55-58, Ranson et al. teach an intermediate trigger signal. However, Ranson et al. don't explicitly disclose a trigger delay providing a sample command a predetermined number of cycles following said intermediate trigger. In column 4, lines 16-31, Tobin et al. disclose a programmable countdown timer that is configured to keep track of the number of clock cycles which pass once its input trigger capture signal is received, and produces a countdown timer enable signal when the number of clock cycles

which have passed equals the programmed clock cycle count. It would have been obvious to one of ordinary skill at the time of the invention to include the countdown timer of Tobin et al. into the system of Ranson et al. A person of ordinary skill in the art would have been motivated to make the modification because *the ability of the debug trigger apparatus to precisely control the signaling delay of the trigger capture signal is critical to allowing the test system to iteratively retrieve continuous yet discrete test node signal events from the integrated circuit in order to form a useful trace of events for use in debugging problems and failures of the integrated circuit* (see Tobin et al.: column 4, lines 25-31).

Referring to claim 5, in column 4, lines 16-18, Tobin et al. disclose the programmable countdown timer may be set to countdown a programmed number of clock cycles before signaling a trigger capture signal (said predetermined number of cycles represent respective operating cycles of the integrated circuit).

Referring to claim 6, in column 4, lines 16-18, Tobin et al. disclose the programmable countdown timer may be set to countdown a programmed number of clock cycles before signaling a trigger capture signal (said predetermined number of cycles represent respective machine clock cycles).

Referring to claim 7, in Figure 8, Tobin et al. disclose a register for the countdown timer (a programmable register storing a value corresponding to said predetermined number of cycles).

Referring to claim 8, in column 3, lines 47-58, Tobin et al. disclose that when an external pulse signal is received, the diagnostics retrieval system may

then reset the integrated circuit, reprogram the trigger condition, and set the programmed delay to a second delay value which is a known increment greater than the first delay value (said programmable register selectively increments said value corresponding to said predetermined number of cycles by a predetermined number of said cycles).

Referring to claim 9, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors the external pulse signal (a sampling circuit responsive to said sample command to identify target data).

Referring to claim 11, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors the external pulse signal (a sampling circuit responsive to said sample command to identify target data).

Allowable Subject Matter

7. Claims 17, 18, and 20 are allowed.

Response to Arguments

8. Applicant's arguments filed May 15, 2007 have been fully considered but they are not persuasive.

9. On page 6, under section **III. Rejections Under 35 U.S.C. § 102**, the Applicant argues, "Figure 4 illustrates a "ring-communication" structure, which is commonly used structure in industry, and it does not teach a FIFO storage array. Rather, the ring allows access to any of the registers therein in any particular order. Applicant attaches two references hereto illustrating and explaining ring

communication structures for further understanding." The Examiner respectfully disagrees. One of the cited references is directed to processor rings, which is not the same as the ring of registers disclosed in Ranson et al. Without particularly pointing out specific pages and lines of the cited reference, the Examiner is unsure as to how the cited reference and the prior art of Ranson et al. are related. Although, the cited U.S. Patent discloses a ring of registers, it doesn't take away from the fact that the remote register of Ranson et al. is a FIFO storage array.

10. On page 6, under section **III. Rejections Under 35 U.S.C. § 102**, the Applicant argues, "This does not teach a FIFO storage array because the relationship between general registers 126 and the ring is not necessarily a First In First Out relationship, since registers 126 can read or write to any of the remote registers in any order." The Examiner disagrees. The claim language describes "a FIFO storage array that stores at least a portion of the sampled data." As stated in the previous Office Action, in Figure 5, Ranson et al. disclose the staging register circuitry. It consists of a header generation register 504 and a staging register 500. Both of these registers are FIFO registers because the bits come in at the top at LOAD/SHIFT and then are shifted serially to the last cell in the register at the bottom and are outputted. Regardless of how each register is addressed, it still doesn't take away from the fact that every register in the ring is a FIFO register. The ring of registers is an array of FIFO registers. The addressing technique discussed by the applicant is to choose a particular register to store the data in, but the register is still a FIFO register as shown in Figure 5.

11. On page 7, under section **III. Rejections Under 35 U.S.C. § 102**, the Applicant argues, "In other words, it appears that the remote registers of figure 4 can be addressed for reads and writes by passing address signals through the ring. Further, rather than shifting data through the registers in a FIFO fashion, as alleged by the office action, it appears that the data is passed from line 412 to 414 not through registers, but through mux 608. Thus, as shown above, a ring communication structure does not teach a FIFO storage array." The Examiner disagrees. When the data is stored in one of the registers, it is stored in a FIFO manner as shown in Figure 5. The data is shifted through the registers. The Applicant has never specifically defined what a FIFO storage array is. It is a reasonable interpretation to say that a FIFO storage array is a register with an array of cells/bits where the data is stored in a FIFO manner. This is the same as the registers in Ranson et al. Further, for sake of argument, if the FIFO storage array were an array of FIFO registers/memory, then the ring of FIFO registers in Ranson et al. would be an array.

12. On page 7, under section **III. Rejections Under 35 U.S.C. § 102**, the Applicant argues, "Further, it does not appear that the figure 4 structure 'stores at least a portion of the sampled data', as required by claim 1. Rather, the remote registers in the ring are control registers with control information. See Col. 11, lines 27-39 and Col. 12, lines 13-17. Therefore, not only do the cited portions fail to teach a FIFO storage array, but the passages also fail to teach an array that stores at least a portion of sampled data." The Examiner disagrees. There are control registers in each of the remote registers that are used to control the

shifting of sampled data through the register. This is evident in column 14, lines 13-25 and in Figure 5.

Conclusion

13. This is an RCE of applicant's earlier Application No. 10/670,620. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is 571-272-3649. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Maskulinski

Michael C Maskulinski
Examiner
Art Unit 2113